Sub C1 B1

11. (New) A method for interfacing between a first component operable at a first clock rate and a second component operable at a second clock rate wherein said second clock rate is higher than said first clock rate, comprising the steps of:

transferring data from said first component to a first buffer operable at said first clock rate;

copying data from said first buffer to a second buffer operable at said second clock rate when said first buffer is substantially full;

prompting said second component to access said data in said second buffer when said copying step is completed.

12. (New) The method as set forth in Claim 11, wherein both said first buffer and said second buffer are shift-register structures.

13. (New) The method as set forth in Claim 11, wherein both said first buffer and said second buffer are random access memories.

14. (New) The method as set forth in Claim 11, wherein said first buffer and said second buffer are both integrated onto the same semiconductor die as one of said first component or said second component.

REMARKS

The claims are claims 1 to 4 and 11 to 14.

Original claims 1 to 10 were subject to a restriction requirement under 35 U.S.C. 121. The OFFICE ACTION states that

this application contains claims directed to the following patentably distinct species:

Species 1 related to Figs. 2 and 3;

Species 2 related to Figs. 4 and 5.

The Examiner requires the Applicant to elect a single disclosed species for prosecution on the merits.

The Applicant made an error in the response filed October 15, 2002 in correlating the species of the Figures cited by the Examiner and the claims. The Applicant now believes that Species 1 related to Figures 2 and 3 were claimed in claims 5 and 6 and Species 2 related to Figures 4 and 5 were claimed in claims 1 to 4 and 7 to 10. Note claim 7 recites "copying data" corresponding to the operation of copy/access control 24 of Figure 4 and "prompting said second component" corresponding to the CONTROL SIGNAL from copy/access control 24 to high clock rate component 22 of Figure 4.

The Applicants elect Species 2 of Figures 4 and 5 without traverse. The Applicants respectfully submit that original claims 1 to 4 and 7 to 10 correspond to this Species 2. Non-elected claims 5 and 6 of Species 1 are canceled. Because original claims 7 to 10 were canceled in the response filed October 15, 2002, these are resubmitted as respective claims 11 to 14.

The Applicants respectfully request early consideration on the merits and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Note inserted text is marked by underlining and deleted text is marked by ~~strikeout~~.

In the Claims

Please amend the claims as follows:

Cancel claims 5 and 6.

Please add new claims 11 to 14 as follows:

11. (New) A method for interfacing between a first component operable at a first clock rate and a second component operable at a second clock rate wherein said second clock rate is higher than said first clock rate, comprising the steps of:

transferring data from said first component to a first buffer operable at said first clock rate;

copying data from said first buffer to a second buffer operable at said second clock rate when said first buffer is substantially full;

prompting said second component to access said data in said second buffer when said copying step is completed.

12. (New) The method as set forth in Claim 11, wherein both said first buffer and said second buffer are shift-register structures.

13. (New) The method as set forth in Claim 11, wherein both said first buffer and said second buffer are random access memories.

14. (New) The method as set forth in Claim 11, wherein said first buffer and said second buffer are both integrated onto the same semiconductor die as one of said first component or said second component.